CLAIMS

What is claimed is:

1. A system for initializing a data processing system, comprising:

a plurality of parameter registers;

a user-defined initialization input defining a first set of initialization data utilized for initializing said data processing system;

a serial non-volatile memory, coupled to said plurality of parameter registers, said serial non-volatile memory utilized for storing a second set of initialization data utilized for initializing said data processing system;

a parallel non-volatile memory, coupled to said plurality of parameter registers, said parallel non-volatile memory utilized for storing a third set of initialization data utilized for initializing said data processing system; and

a multiplexor interposed between said parameter registers and said user-defined initialization input, said serial non-volatile memory, and said parallel non-volatile memory for determining a selection from said user-defined initialization input, said serial non-volatile memory, and said parallel non-volatile memory and relaying said selection to said plurality of parameter registers, in response to a control signal.

2. The system for initializing a data processing system according to claim 1, further including a set of control resistors coupled to a user-defined control input, wherein said set of control resistors outputs said control signal in response to said user-defined control input.

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3. The system for initializing a data processing system according to claim 1, further including a set of initialization resistors coupled to a user-defined initialization input, wherein said set of initialization resistors outputs an initialization signal, in response to said user-defined initialization input.

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4. The system for initializing a data processing system according to claim 1, further including a command decoder is interposed between said multiplexor and said processor and said parallel non-volatile memory, said command decoder is utilized for filtering commands issued from said processor for a set of desired commands.

5. The system for initializing a data processing system according to claim 1, further including a serial non-volatile memory controller is interposed between said serial non-volatile memory and said multiplexor, said serial non-volatile memory controller is utilized for controlling data sent from serial non-volatile memory.

6. The system for initializing a data processing system according to claim 1, further including a parallel non-volatile memory controller is interposed between said parallel non-volatile memory and said command decoder, said parallel non-volatile memory controller is utilized for controlling data sent from parallel non-volatile memory.

7.   A data processing system, comprising:

a processor;

a memory, coupled to said processor; and

a system for initializing a data processing system, comprising:

a plurality of parameter registers;

a user-defined initialization input defining a first set of initialization data utilized for initializing said data processing system;

a serial non-volatile memory, coupled to said plurality of parameter registers, said serial non-volatile memory utilized for storing a second set of initialization data utilized for initializing said data processing system;

a parallel non-volatile memory, coupled to said plurality of parameter registers, said parallel non-volatile memory utilized for storing a third set of initialization data utilized for initializing said data processing system; and

a multiplexor interposed between said parameter registers and said user-defined initialization input, said serial non-volatile memory, and said parallel non-volatile memory for determining a selection from said user-defined initialization input, said serial non-volatile memory, and said parallel non-volatile memory and relaying said selection to said plurality of parameter registers, in response to a control signal.

8.   A host data processing system, comprising:

an integrated circuit in which a data processing system in accordance with claim 7 is fabricated;

an interconnect coupled to said integrated circuit;

a host processor; and

a host memory.

9.   A method of initializing a data processing system, comprising:

sending a control signal to a multiplexor, said control signal designating one of a plurality of sets of initialization data as a preferred set of initialization data;

relaying said preferred set of initialization data to a plurality of parameter registers; and

utilizing said preferred set of initialization data stored in said plurality of parameter registers to initialize said data processing system.

10.   The method of initializing a data processing system according to claim 9, further including:

generating a signal, by a user, from a user-defined control input to send said control signal to said multiplexor.

11.   The method of initializing a data processing system according to claim 9, further including:

filtering commands by a command decoder, said commands issued from a processor, in response to designating a set of initialization data stored in a parallel non-volatile memory as said preferred set of initialization data.

12.   The method of initializing a data processing system according to claim 9, further including:

designating a initialization signal sent from a n initialization input as said preferred set of initialization data, in response to selecting a first option by said control signal.

13.   The method of initializing a data processing system according to claim 9, further including:

designating a set of initialization data stored in a serial non-volatile memory as said preferred set of initialization data, in response to selecting a second option by said control signal.

14.   The method of initializing a data processing system according to claim 9, further including:

designating a set of initialization data stored in a parallel non-volatile memory as said preferred set of initialization data, in response to selecting a third option by said control signal.